

What is claimed is:

- 1 1. A circuit comprising:
2 a first driver to receive a first signal from a first input port;
3 a second driver to receive a time-delayed version of the first signal from a second
4 input port; and
5 a transformer coupled to the first driver and the second driver, the transformer to
6 provide an output signal to an output port.
- 1 2. The circuit of claim 1, further comprising a capacitive load coupled to the
2 transformer.
- 1 3. The circuit of claim 2, wherein the transformer has a leakage inductance and the
2 capacitive load has a capacitance, and the time-delayed version of the first signal is time-
3 delayed with respect to the first signal by a time about equal to a product of π and a
4 square-root of a product of the leakage inductance and the capacitance.
- 1 4. The circuit of claim 1, further comprising an inductor coupled to the transformer
2 and a transistor coupled to the inductor.
- 1 5. The circuit of claim 4, wherein the inductor has an inductance and the transistor
2 has a capacitance and the time-delayed version of the first signal is time-delayed with
3 respect to the first signal by a time about equal to a product of π and a square-root of a
4 product of the inductance and the capacitance.
- 1 6. The circuit of claim 1, further comprising a Schmitt trigger circuit to couple the
2 output port to the second input port.

- 1 7. The circuit of claim 6, wherein the Schmitt trigger circuit includes a hysteresis
2 value about equal to a supply potential.
- 1 8. The circuit of claim 7, further comprising a clamp circuit coupled to the output
2 port, the clamp circuit to hold the output port at the supply potential.
- 1 9. An apparatus comprising:
2 a plurality of circuits, each of the plurality of circuits including a plurality of
3 drivers coupled to a first transformer circuit, wherein the first transformer circuit in each
4 of the plurality of circuits is coupled to a second transformer circuit including a center-tap
5 and each of the plurality of drivers in each of the plurality of driver circuits is coupled to
6 a separate input port.
- 1 10. The apparatus of claim 9, wherein the first transformer circuit in at least one of
2 the plurality of driver circuits comprises a loosely coupled transformer.
- 1 11. The apparatus of claim 10, further comprising a capacitive load coupled to the
2 center- tap.
- 1 12. The apparatus of claim 11, wherein the capacitive load comprises a
2 complementary metal-oxide field-effect transistor.
- 1 13. The apparatus of claim 9, wherein the second transformer comprises an auto-
2 transformer.
- 1 14. An apparatus comprising:
2 a communication circuit formed on a substrate; and
3 a power supply circuit formed on the die to provide power to the communication
4 circuit, the power supply circuit including:
5 a first driver coupled to an input port;
6 a delay circuit coupled to the input port;

7 a second driver coupled to the delay circuit; and
8 an auto-transformer coupled to the first driver, to the second driver, and to
9 an output port, the output port being coupled to a capacitive load and the
10 capacitive load being coupled to the communication circuit to provide power to
11 the communication circuit.

1 15. The apparatus of claim 14, wherein the communication circuit comprises a
2 communication base station.

1 16. The apparatus of claim 15, wherein the transformer includes a leakage inductance,
2 the capacitive load includes a capacitance, and the delay circuit includes a delay about
3 equal to a product of π and the square-root of a product of the leakage inductance and the
4 capacitance.

1 17. The apparatus of claim 16, wherein the processor comprises a reduced instruction
2 set processor.

1 18. The apparatus of claim 14, further comprising a processor coupled to the
2 communication circuit.

1 19. The apparatus of claim 18, wherein the processor comprises a very-long
2 instruction word processor.

1 20. A method comprising:
2 receiving a first input signal;
3 receiving a second input signal, the second input signal being a time-delayed
4 version of the first input signal; and
5 processing the first input signal and the second input signal to generate a half-
6 raised cosine signal.

- 1 21. The method of claim 20, wherein receiving the first input signal comprises
2 receiving a digital signal.
- 1 22. The method of claim 21, wherein receiving the second input signal comprises
2 receiving a digital signal.
- 1 23. The method of claim 22, wherein processing the first input signal and the second
2 input signal comprises providing a signal path including a first driver, an inductor, and a
3 capacitive load for the first input signal and a signal path including a second driver, the
4 inductor, and the capacitive load for the second input signal.
- 1 24. The method of claim 20, wherein receiving the first input signal comprises
2 receiving a low-to-high transition signal.